## REMARKS

In the July 31, 2002 Office Action Summary, the Examiner objects to the Applicant's drawings and rejects all claims pending in the application (Claims 1-36). The Applicant submits the below arguments in response. In addition, new Claims 37-44 are submitted for consideration.

Applicant requests a clarification on the drawing request since Figures 1 and 4 to 7 are cross sectional views and Figures 2 and 3 are graphs. What unlabeled boxes are at issue?

In one aspect, the present invention is directed toward an improved semiconductor laser with improved laser characteristics, such as a lowered threshold current. In particular, the invention takes advantage of the inverse relationship which exists between the progression of horizontal etching (occurring during thermal cleaning) and the concentration of carriers in the current blocking layer of the semiconductor laser device. In Figure 2, the extent to which the horizontal etching progresses is inversely correlated to the concentration of carriers in the current blocking layer as shown. That is, the lower the concentration of carriers in the current blocking layer the slower the horizontal etching will progress.

As shown in the prior art Figure 7, horizontal etching which occurs at the joins between the current blocking layer and the p-type cladding layer creates conclaves in the current blocking layer leaving hollows in the overall laser structure (shown by character reference 12). These hollows cause wave-guide loss in the semiconductor laser which worsens semiconductor laser light transmission due to the raised threshold current.

To suppress the horizontal etching at the joins between the current blocking layer and the p-type cladding, the current blocking layer of the present invention is formed with at least two regions having different concentrations of n-type carriers (N1 and N2, where $N1<N2$). The region of the current blocking layer nearest the p-type cladding is formed having a N1 concentration while a part or all of the remaining portion of the current blocking layer is formed having a p-type carrier concentration of N2. The overall conductivity of the current blocking layer is n-type.

By lowering the concentration of carriers in the portion of current blocking layer

nearest the p-type cladding, the present invention suppresses the etching at the joins and substantially eliminates the existence of the hollows. This in turn, lowers the threshold current of the laser and raises the laser slope efficiency, thereby improving the laser characteristics.

The Office Action rejected Claims 1 and 15-29 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,776,792 issued to Naito et al. (the "Naito patent"). In particular, the Naito patent discloses a method for forming a semiconductor laser device comprising a n-type semiconductor substrate, n-type cladding, and active layer, a p-type cladding, a p-type buried cladding, and a current blocking layer. The Office Action noted that the Naito patent purportedly showed a p-type buried cladding layer having a refractive index higher than the current blocking layer. Applicant respectfully traverse this rejection.

Naito generally discusses as prior art, a current blocking layer of a high-resistivity formed on either side of the active layer which causes abrupt confinement of laser light due to the difference in refractive index between the active layer and the high resistivity layer. The Naito patent has a requirement that a stripe region be etched in the semiconductor device to form a preferably thin n-type current blocking region to facilitate the production of a semiconductor laser structures. However, as the Naito patent discloses, the controlling the width of the stripe is critical since variations in the stripe width result in lowered semiconductor yield.

Naito proposes eliminating the problem of controlling the stripe width by providing a semiconductor laser structure having a flat surface without the use of a current blocking layer (see e.g., the Naito patent, Col. 4, Lines 44-56, Col. 5, Lines 20-30). To achieve this result, the Naito patent proposes controlling the stripe width by increasing the resistance of the region outside the stripe through manipulation of the refractive index of the layers surrounding the stripe region.

In contrast to the Naito patent, the Applicant's invention solves the problem of hollows produced by horizontal etching performed during thermal cleaning. Thus, the Naito patent solves a different problem than does Applicant's invention. Further, Applicant can find no mention in the Naito patent of a current blocking layer containing at least two regions, wherein the regions have different carrier concentrations as is

claimed by Applicant. Indeed, the Natio patent proposes to eliminate the need for a current blocking region altogether.

Consequently, Applicant respectfully submit that the Naito patent neither claims nor discloses all the elements of the Applicant's invention. The Naito patent is, therefore, an improper reference for sustaining a proper 35 U.S.C. §102 rejection. Applicant requests that the rejection of Applicant's claims in light of the Naito patent be withdrawn, and that favorable reconsideration be given in light of the Applicant's arguments.

The Office Action rejects Claims 2-4, 7-10, 25-28 and 31-34 under 35 U.S.C. §103(a) as being unpatentable over the Naito patent in view of U.S. Patent No. 6,363,506B1 issued to Hata (the "Hata patent"). In particular, the Office Action posits that the Naito patent discusses all the elements of the Applicant's invention except the concentration of n-type carriers in the first and second layers [of the current blocking layer] being N1 and N2. The Office Action suggests that the Hata patent discloses that the first and second layers have different compositions of n-type N1 and N2.

Applicant notes that the effective prior art date of the Hata patent is November 23, 1999. The present invention claims priority from its Japanese Document No 11-55021 dated March 3, 1999. Thus, the effective date of present invention predates the Hata patent. However, without submitting an English translation of the priority document, the Hata patent is still not relevant to the present claims.

The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into a primary reference's structure, but rather what the combined teachings of the references would suggest to those of ordinary skill in the art. In re Keller, 642 F.2d 413, 425 (C.C.P.A. 1981).

The Hata patent generally discloses a semiconductor structure having a reflective layer which reflects the light generated in the light-emitting layer toward the device substrate. The reflective layer is formed between the light emitting layer and a device electrode. The reflective layer is a multilayer film including at least two different types of layers which are alternately deposited on one another, wherein the layers have different refractive indexes and thicknesses (see e.g., the Hata patent, Col. 3, Lines 1-10). The Hata patent further discloses a semiconductor layer including at least a pair of cladding layers with a light-emitting layer formed there between (see e.g., the Hata

patent, Col. 3, Lines 11-31).

Applicant notes that the Hata patent is directed toward a semiconductor laser with improved light transmission due to the respective thicknesses of the layers comprising the multilayer film (see e.g., the Hata patent, Col. 4, Lines 15-50). In accordance with the Hata patent, the two differing thicknesses prevent the light generated in the light-emitting layer from being absorbed and scattered by the electrode. Further, the layers of the multilayer film in the Hata patent are preferably doped with a p-type impurity or an n-type impurity in order to facilitate the passage of an externally injected current. The multilayer film includes about 10-100 pairs of such differently doped semiconductor layers.

The Hata patent does not disclose, claim or suggest a current blocking layer having at least two regions as is claimed by the Applicant. In particular, the Hata patent does not disclose a current blocking layer having different regions including differing concentrations of carriers. Thus, since neither the Naito patent nor the Hata patent disclose, suggest or claim the elements of the Applicant's invention singularly or in combination, it is improper to combine the references to sustain a 35 U.S.C. §103 rejection of the Applicant's claims. In addition, any hypothetical combination of the Naito patent with the Hata patent would not arrive at the Applicant's invention.

The Office Action further rejects claims 11-14 and 35-36 under 35 U.S.C. §103(a) as being unpatentable over the Naito patent in view of U.S. Patent No. 4,800,565 issued to Yoshizawa et al. (the "Yoshizawa patent"). Applicant respectfully traverse this rejection.

The Yoshizawa patent discloses generally a semiconductor layer wherein an interface layer is provided on an upper cladding formed on an active layer. The Yoshizawa patent is directed toward solving the problem of astigmatism which results from the oxidation of the cladding layer which is exposed to air during the formation of the channel stripe. The oxidation causes the yield of the semiconductor device to be undesirable low (see e.g., Yoshizawa, Col. 1, Lines 22-45).

The Yoshizawa patent proposes to solve the oxidation problem by manipulating the Al mole ratio of a semiconductor layer which defines the bottom of the channel stripe. The Al mole ratio of the stripe channel bottom is set smaller than that of the cladding

layer and is smaller than or equal to the Al mole ratio of the active layer. Alternatively, the Al mole ratio of the semiconductor layer constituting the bottom of the channel stripe is formed so that the Al mole ratio is smaller that that of the semiconductor layer constitution the cladding layer and the refractive index of the buried cladding layer is set smaller than the refractive index of the cladding layer. Further still, the Al mole ratio of the semiconductor layer constituting the channel stripe is formed with an Al mole ratio smaller than that of the cladding layer but larger than that of the active layer (see e.g., Col. 1-Col. 2, Line 7). In this way, the Yoshizawa patent suggests that since the semiconductor constituting the interface laser has a wider band gap than that of the active layer, then there is no absorption loss caused by the bottom portion of the stripe channel. Further, by varying the Al mole ratio in this manner, no oxidation is formed in the stripe channel.

Neither the Yoshizawa patent nor the Naito patent discuss, suggest or claim a current blocking layer including two regions of differing carrier concentrations. Further, the references do not disclose a interjacent layer being deposited between the current blocking layer and a p-type cladding base layer with the lower surface of the current blocking layer separated from an upper surface of the p-type cladding layer as claimed by the Applicant. Consequently, taken singularly or in combination, the Naito patent and the Yoshizawa patent do not suggest, claim or disclose the Applicant's invention. In addition, Applicant can find no motivation to combine the references in the references themselves. Further still, should the Naito patent and the Yoshizawa patent be combined, the Applicant's invention would not be obtained. Therefore, the Applicant submits that the Naito patent combined with the Yoshizawa patent does not support a 35 U.S.C. §103 rejection.

Applicant respectfully points out that none of the references cited in the Office Action teach the source of the problem solved by Applicant. Absent recognition of the problems faced and solved by Applicant, the prior art cannot suggest singularly or in combination a solution as novel as Applicant's invention. Eibel Process Co. v. Minnesota and Ontario Paper Co., 261 U.S. 45 (1923).

Applicant respectfully asserts that all of the claims pending in the application (e.g., Applicant's independent claims and the dependent claims that depend variously

therefrom) are in condition for allowance. If there are any questions in connection with entry of this Amendment, please contact the undersigned attorney.

Should the Examiner wish to discuss any of the above in greater detail or deem that further amendments should be made to improve the form of the claims, then the Examiner is invited to telephone the undersigned at the Examiner's convenience.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231 on October 23, 2002.

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Signature

Date: October 23, 2002

Respectfully submitted,

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